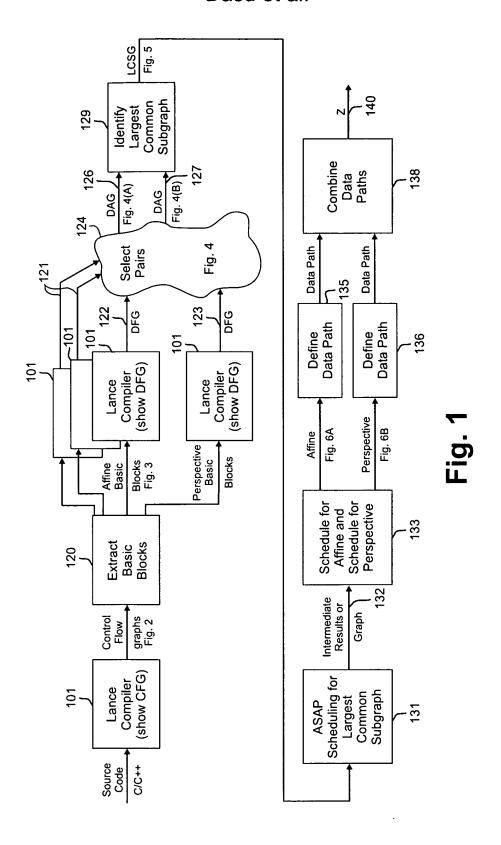
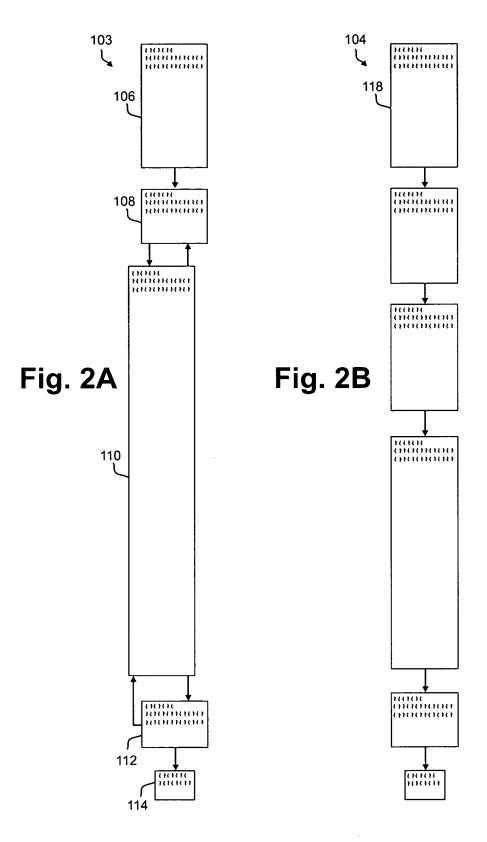
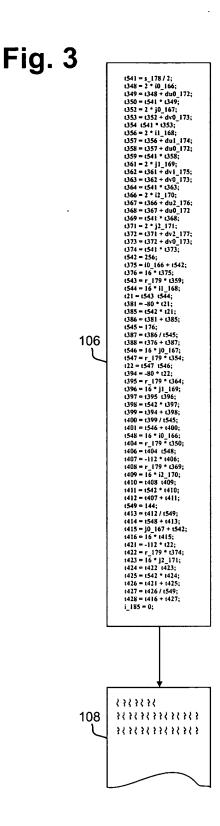
# Reconfigurable Processing 10/544894 Dasu et al.



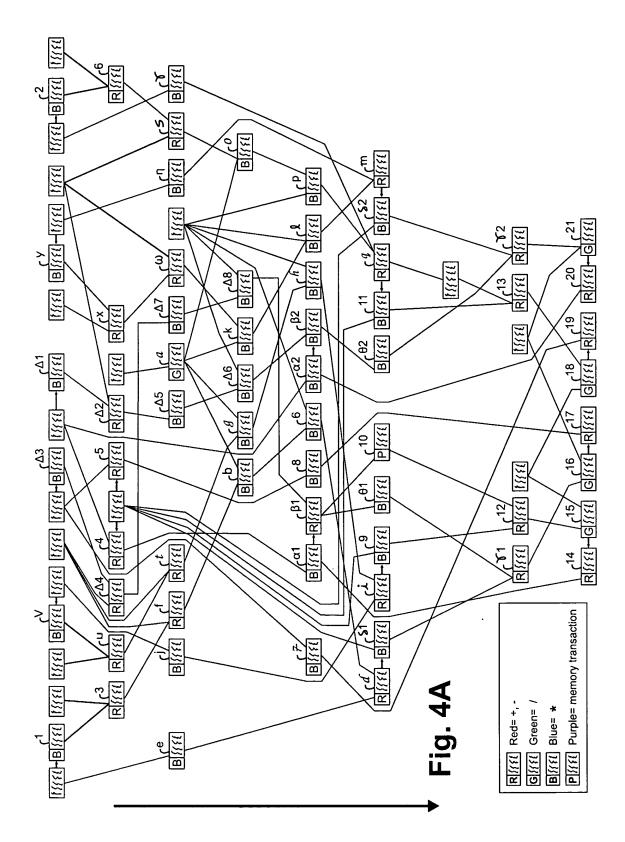
# Reconfigurable Processing 10/544894 Dasu et al.



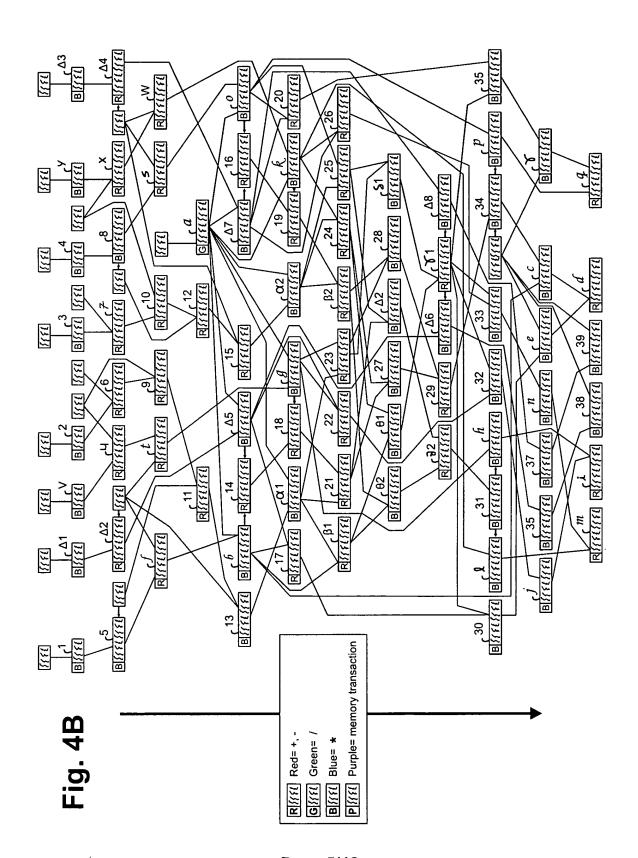
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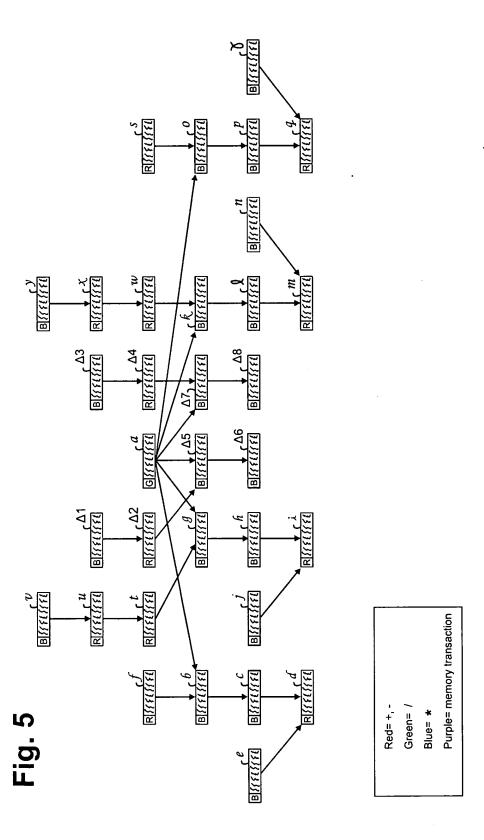
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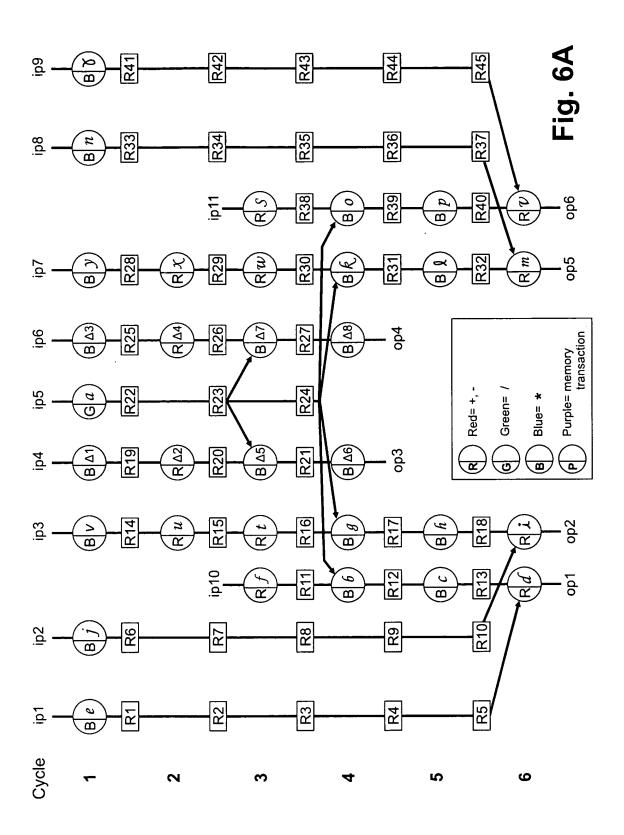
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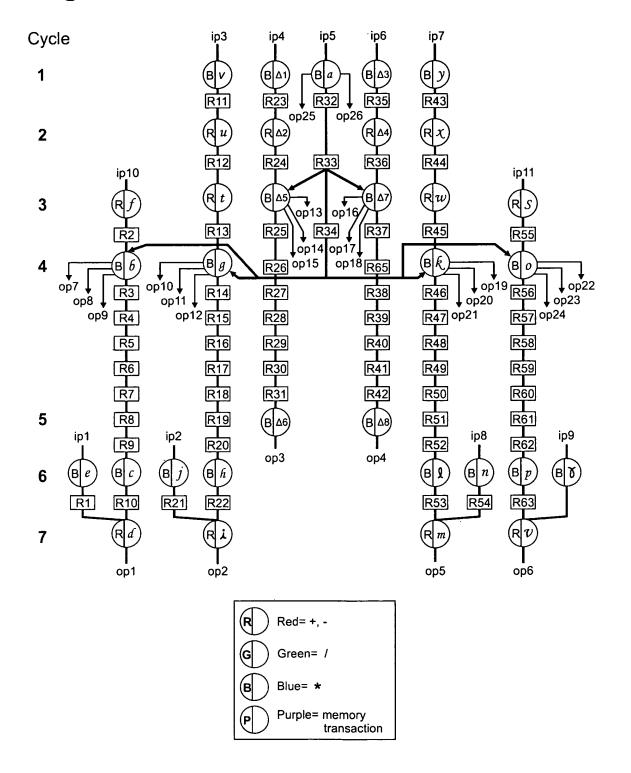
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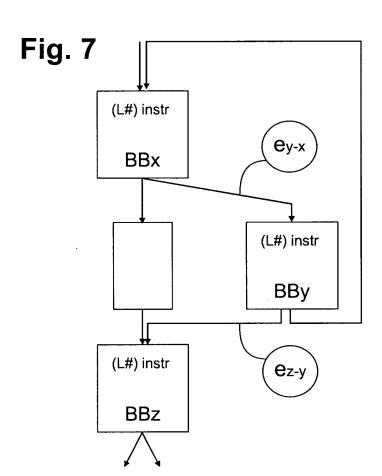


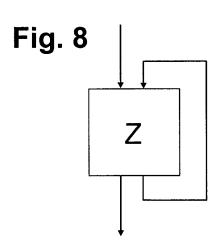
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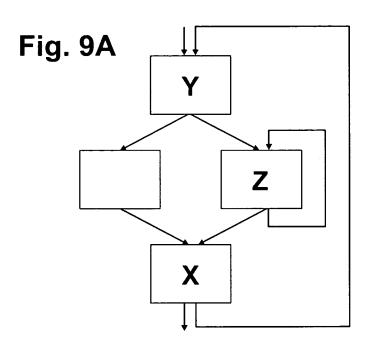
#### Fig. 6B

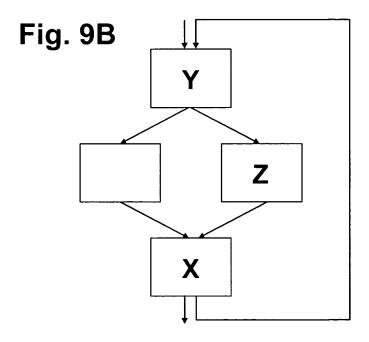




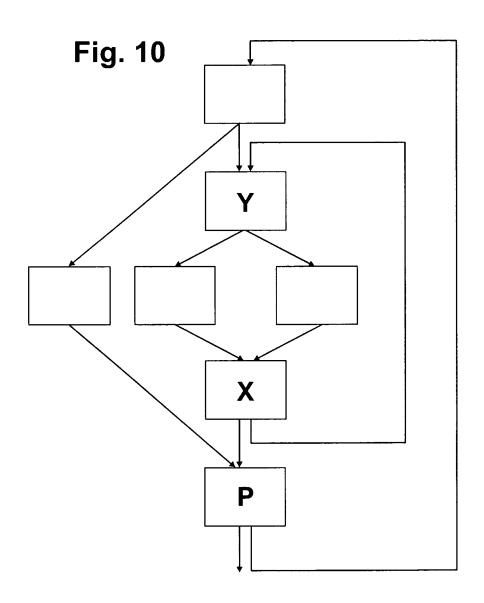


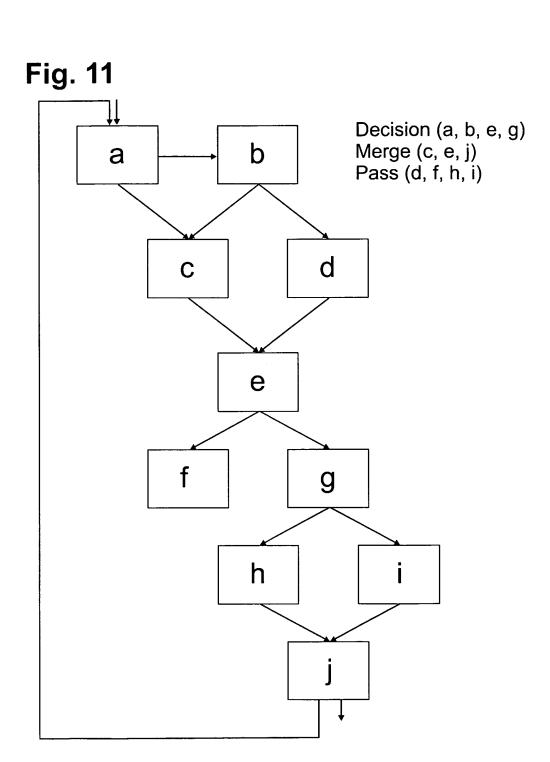
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Fig. 12

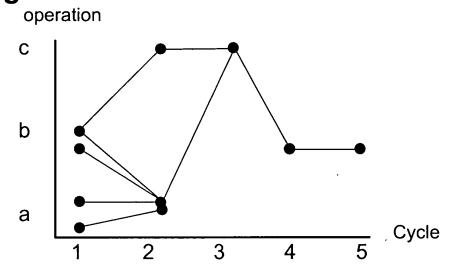


Fig. 12A

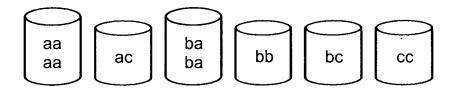


Fig. 13

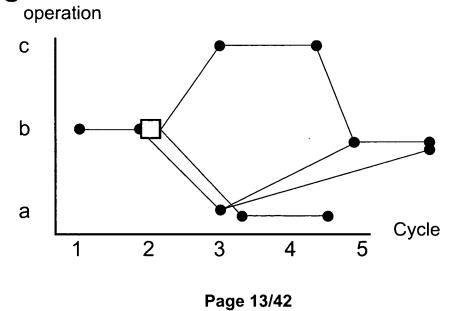


Fig. 13A

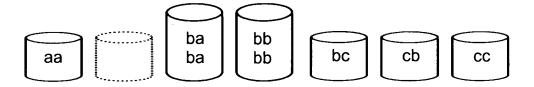


Fig. 14A

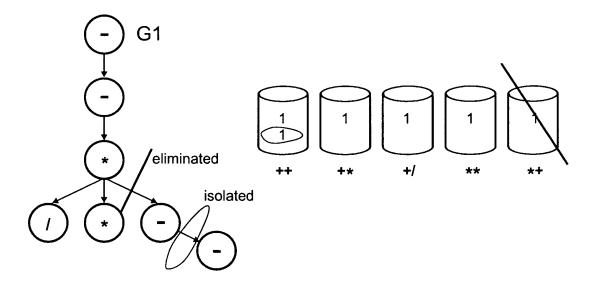
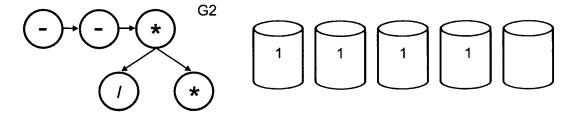
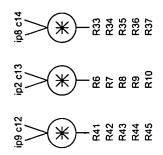
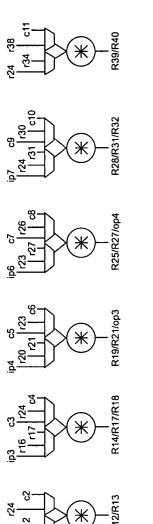
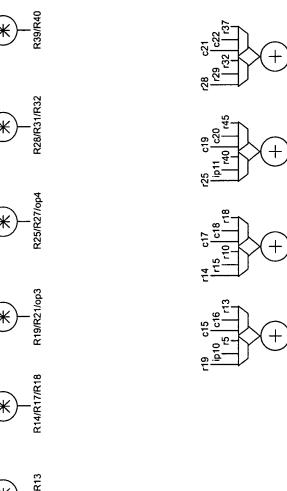


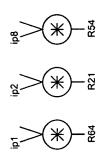
Fig. 14B

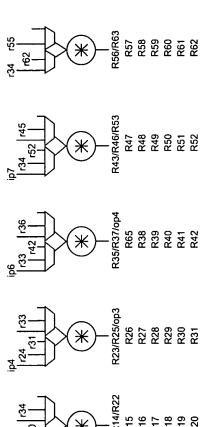


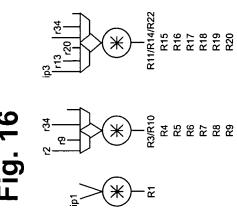


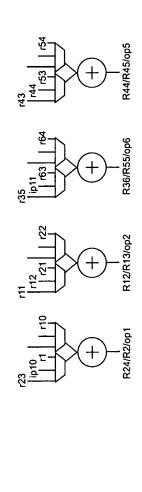




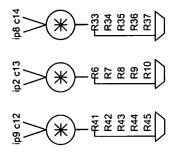


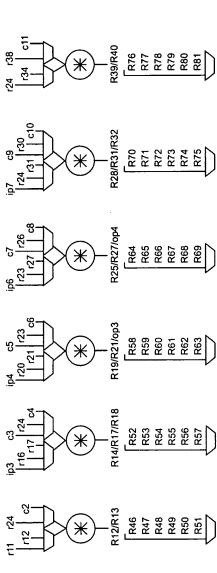


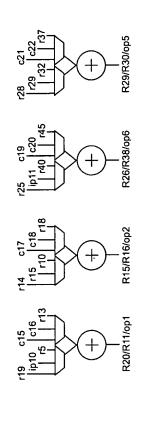


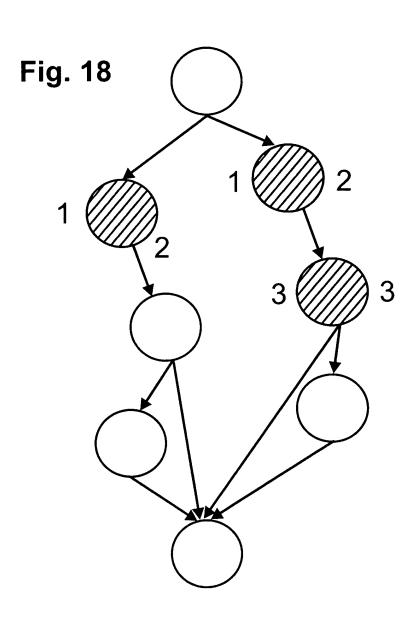


# Reconfigurable Processing United 4893









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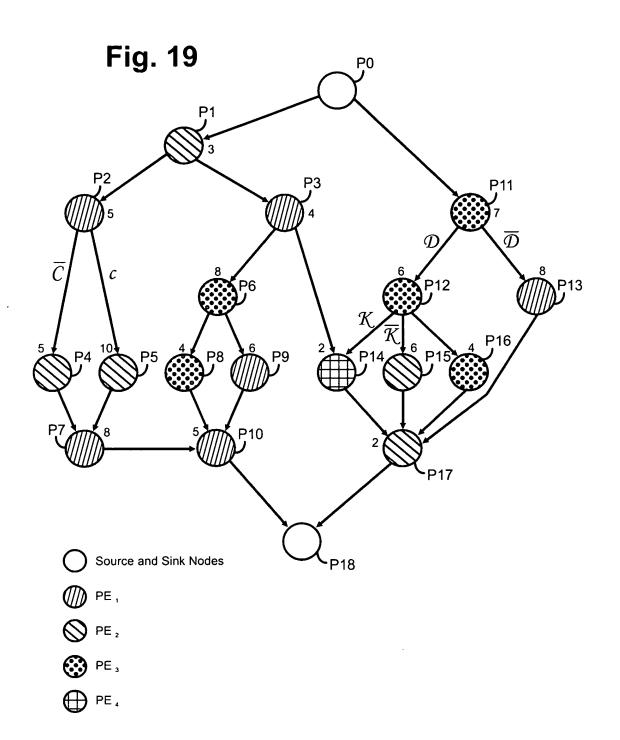
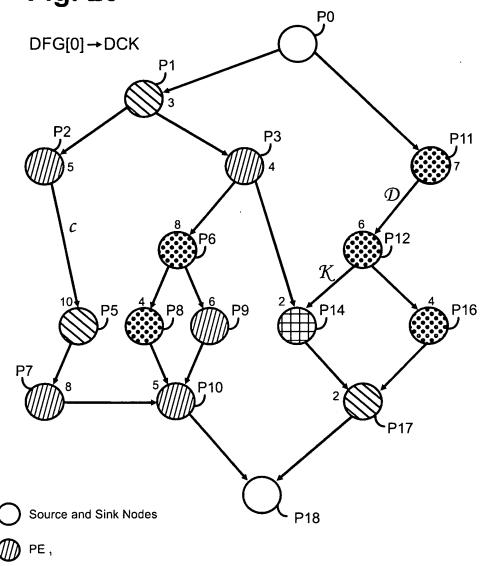


Fig. 20

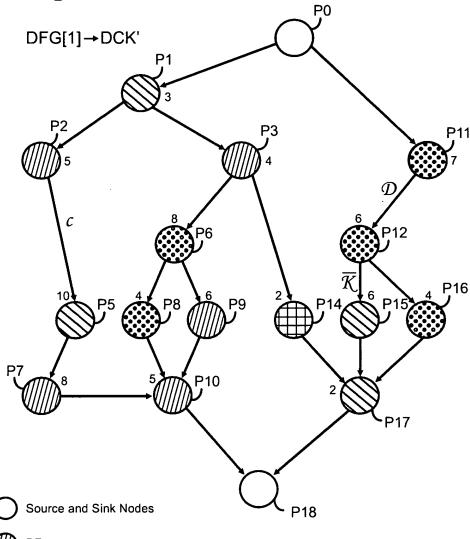


PE,

PE,

PE.

Fig. 21



- (M) PE.
- PE 2
- PE 3
- PE 4

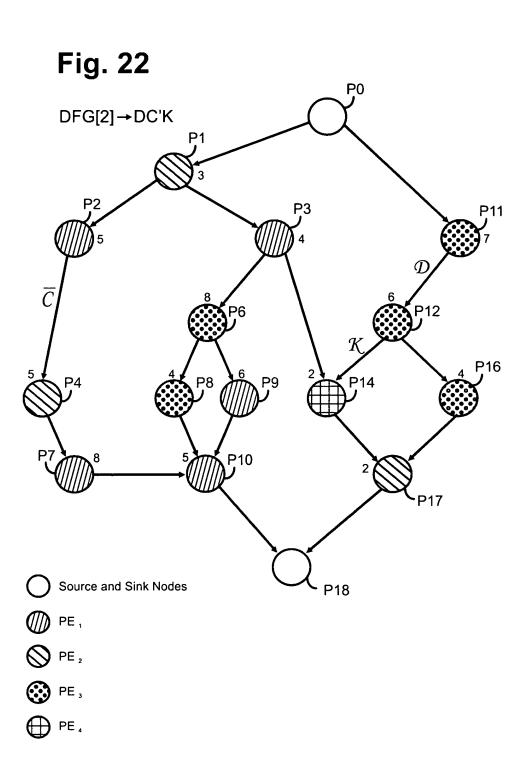
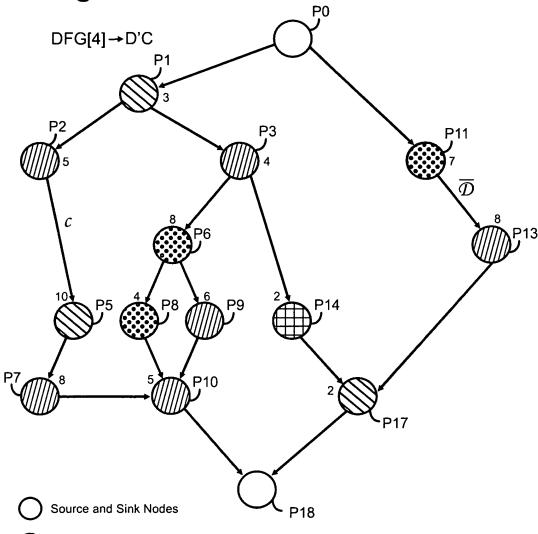


Fig. 23 P0 DFG[3]→DC'K' Р3 P10 P17 Source and Sink Nodes P18 PE, PE 2 PE 3 PE 4





- (M) PE,
- PE,
- PE 3
- ◆ PE 4

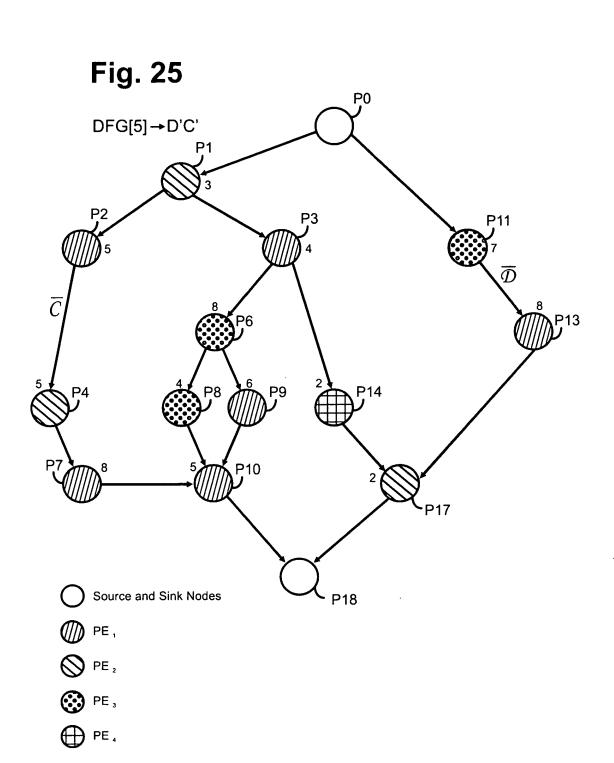


Fig. 26

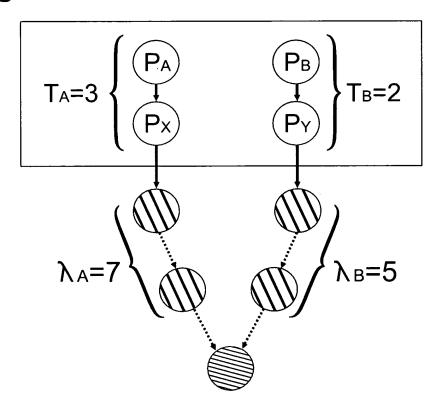
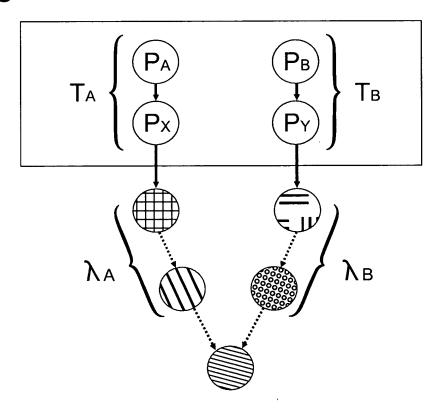
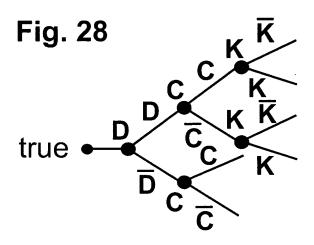
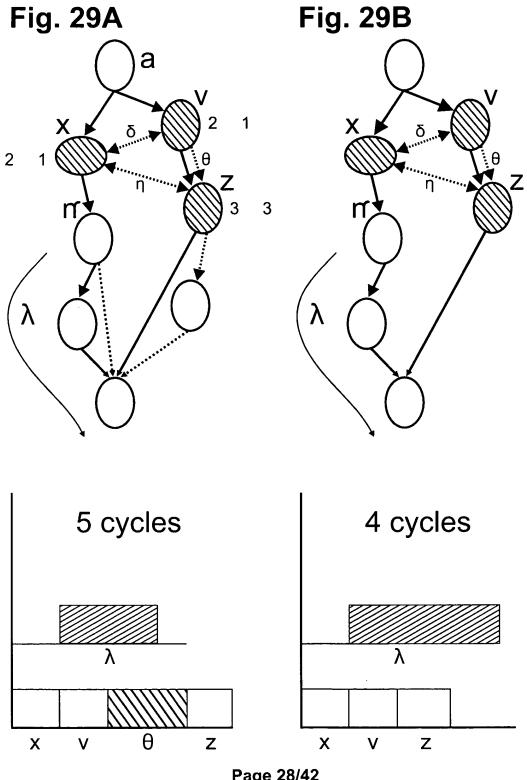


Fig. 27

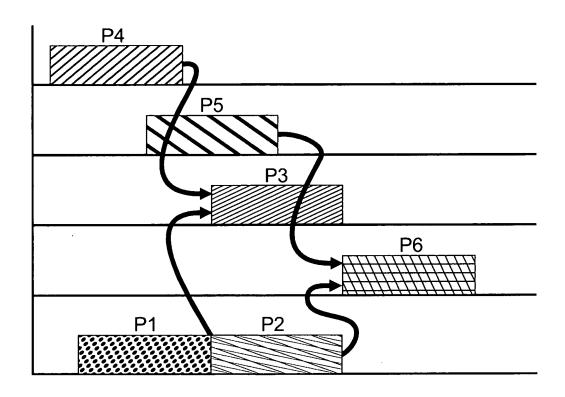






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Fig. 30



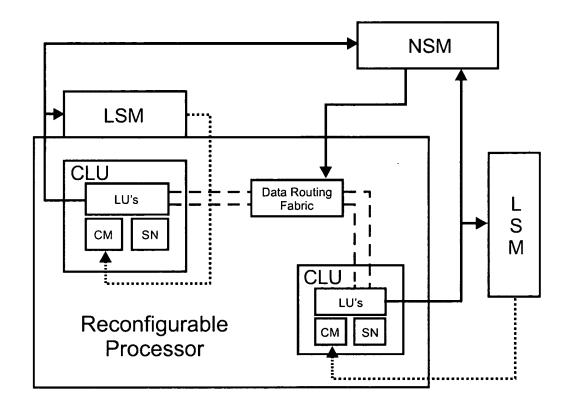
#### Fig. 31

	Expression α	Expression β	Expression θ	Expression Υ
Process A		0		
Process B		10		

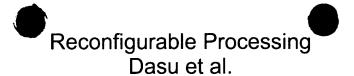
	Expression α	Expression β	Expression θ	Expression Y
Process A		30		
Process B		40		

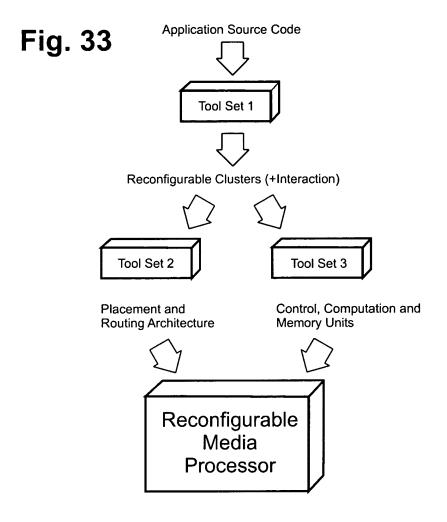
and so on

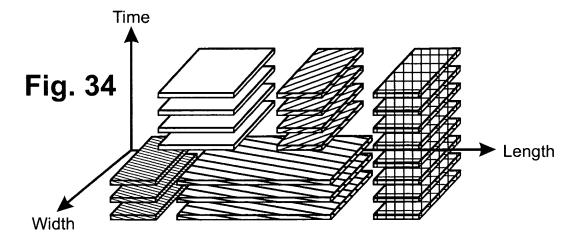
Fig. 32



CLU=Configurable Logic Unit LU=Logic Units SN=Switching Network CM=Configuration Memory LSM=Logic Schedule Manager NSM=Network Schedule Manager



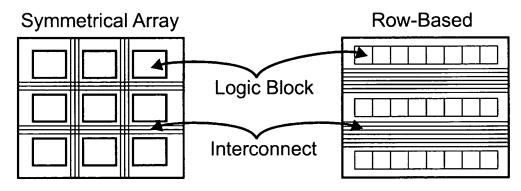




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Fig. 35

#### Routing Architecture Overview



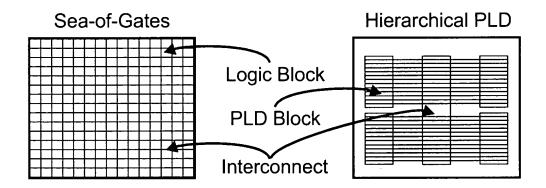
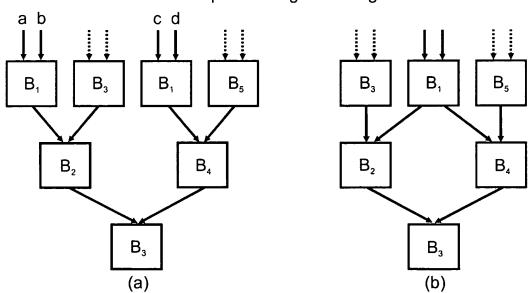


Fig. 36

Multiple vs. Single Building Block



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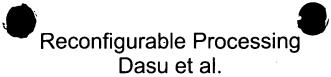
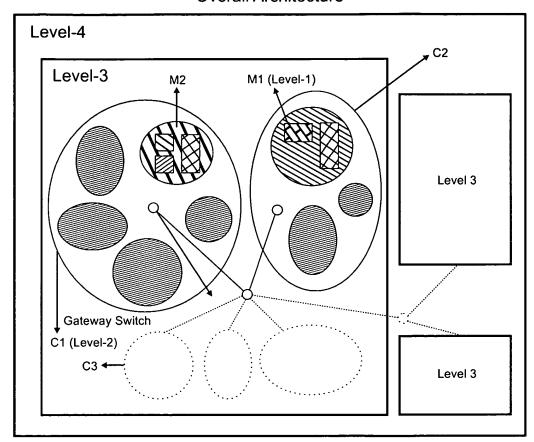
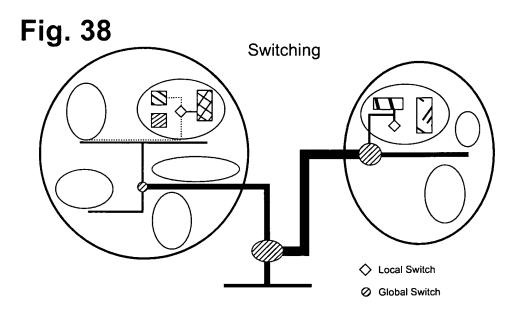


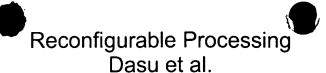
Fig. 37

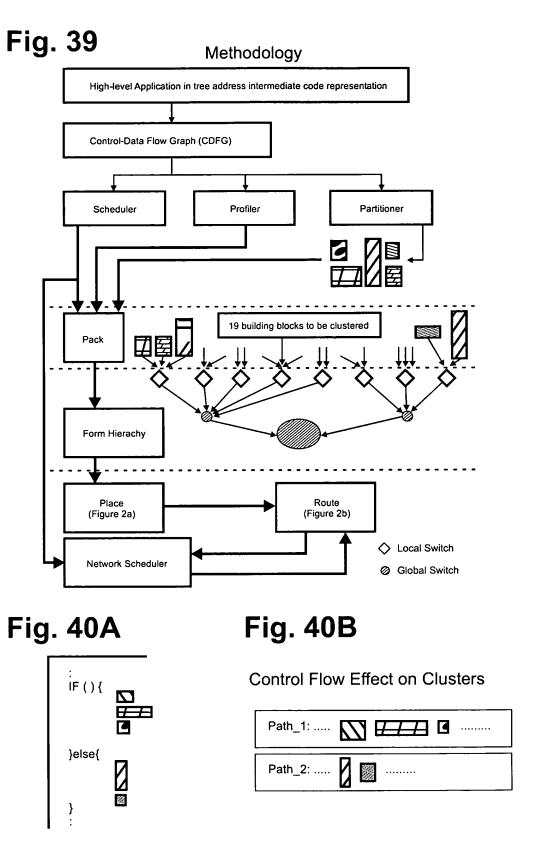
#### **Overall Architecture**





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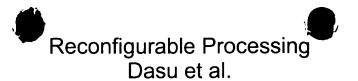


Fig. 41A

**Cost Matrix** 

	Α	В	С	D	Ε	F
Α	0	X	X	Х	Х	X
В	5	0	Х	Х	Х	X
С	6	0	0	Х	Х	Х
ם	4	3	7	0	Х	Х
Ε	1	4	1	0	0	Х
F	3	0	4	5	3	0

Fig. 41B

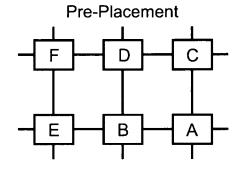
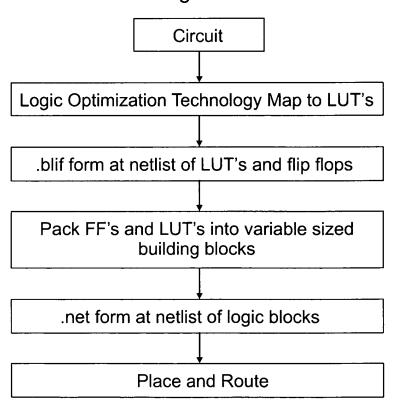


Fig. 42

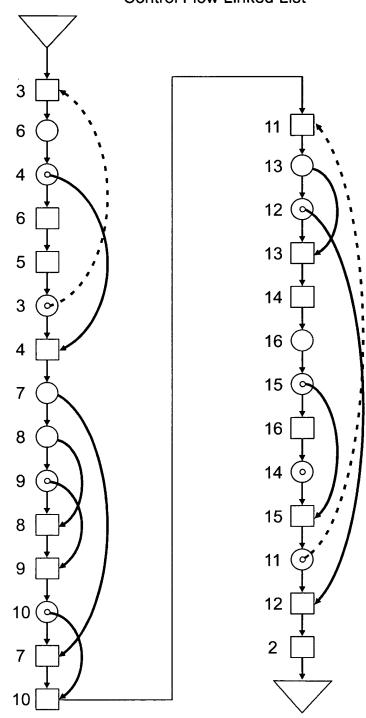
**Design Flow** 



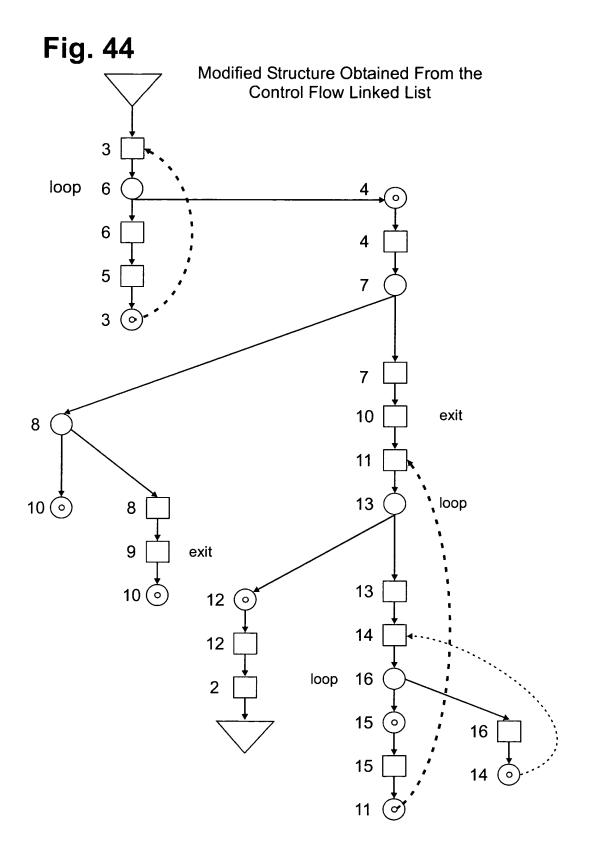
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Fig. 43

Control Flow Linked List

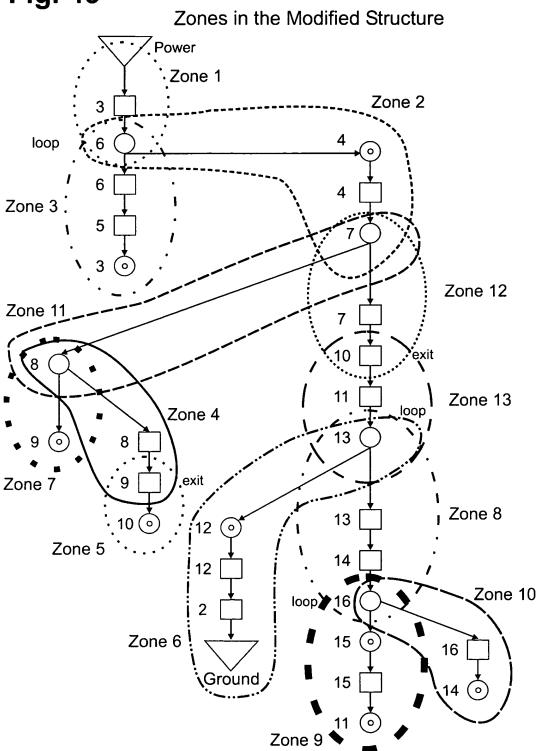






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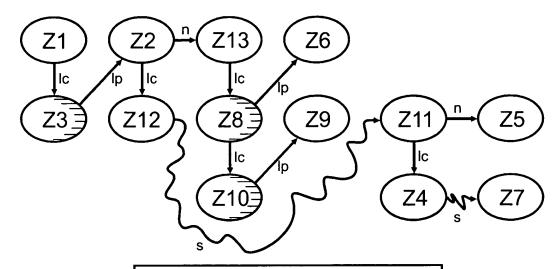
Fig. 45



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Fig. 46

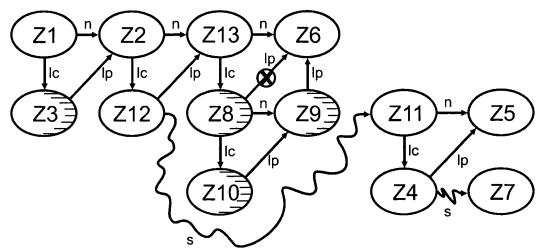
#### Initial Zone Structure Obtained



- s: sibling relationship
- lc: later child relationship
- lp: later parent relationship
- In all types, destination zone is (lc/s/lp) of source zone. The shaded zones are Loop types.

Fig. 47

#### Comprehensive Zone Structure with Cancelled Links Shown



- s: sibling relationship
- Ic: later child relationship
- lp: later parent relationship
- In all types, destination zone is (lc/s/lp) of source zone.
- The shaded zones are Loop types.

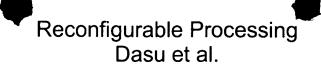
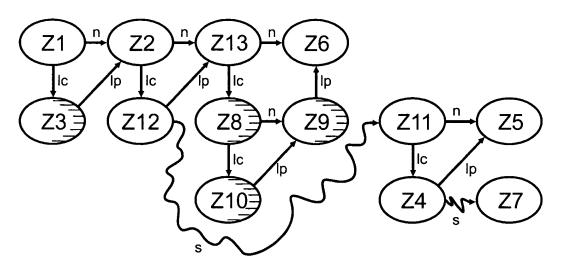


Fig. 48

Comprehensive Zone Structure with Cancelled Links Removed



s: sibling relationship

Ic: later child relationship

lp: later parent relationship

In all types, destination zone is (lc/s/lp) of source zone.

The shaded zones are Loop types.

Fig. 49

#### **Sequentially Ordered Zones**

